DATA SHEET

TDA5737A
5 V VHF, hyperband and UHF mixers/oscillators for TV and VCR 3-band tuners

Preliminary specification
Supersedes data of 2000 Nov 08
File under Integrated Circuits, IC02

2000 Dec 19

Philips
Semiconductors

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FEATURES

- Balanced mixer with a common emitter input for band A (single input)
- 2-pin oscillator for band A
- Balanced mixer with a common base input for bands B and C (balanced input)
- 3-pin oscillator for band B
- 4-pin oscillator for band C
- Local oscillator buffer output for external prescaler
- SAW filter preamplifier with a low output impedance to drive the SAW filter directly
- Band gap voltage stabilizer for oscillator stability
- Electronic band switch
- External IF filter between the mixer output and the IF amplifier input.

GENERAL DESCRIPTION

The TDA5737A is a monolithic integrated circuit that performs the mixer/oscillator functions for bands A, B and C in TV and VCR tuners. This low power mixer/oscillator requires a power supply of 5 V and is available in a very small package.

This device gives the user the capability to design an economical and physically small 3-band tuner.

It is suitable for European standards, as illustrated in Fig.16, with the following RF bands: 48.25 to 168.25 MHz, 175.25 to 447.25 MHz and 455.25 to 855.25 MHz. With an appropriate tuned circuit, it is also suitable for NTSC all channel tuners (USA and Japan).

The tuner development time can be drastically reduced by using this device.

APPLICATIONS

- 3-band all channel TV and VCR tuners
- Any standard.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		–	5.0	–	V
I_P	supply current		–	50	–	mA
$f_{i(RF)}$	RF input frequency	band A; note 1	41	–	171	MHz
		band B; note 1	166	–	451	MHz
		band C; note 1	446	–	861	MHz
G_v	voltage gain	band A	–	23	–	dB
		band B	–	34	–	dB
		band C	–	34	–	dB
NF	noise figure	band A	–	7.5	–	dB
		band B	–	8	–	dB
		band C	–	9	–	dB
V_o	output voltage level causing 1% cross modulation in channel	band A	–	116	–	dBμV
		band B	–	115	–	dBμV
		band C	–	115	–	dBμV

Note

1. The limits are related to the tank circuits used in Fig.16 and the intermediate frequency. Frequency bands may be adjusted by the choice of external components.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5737ATS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

BLOCK DIAGRAM

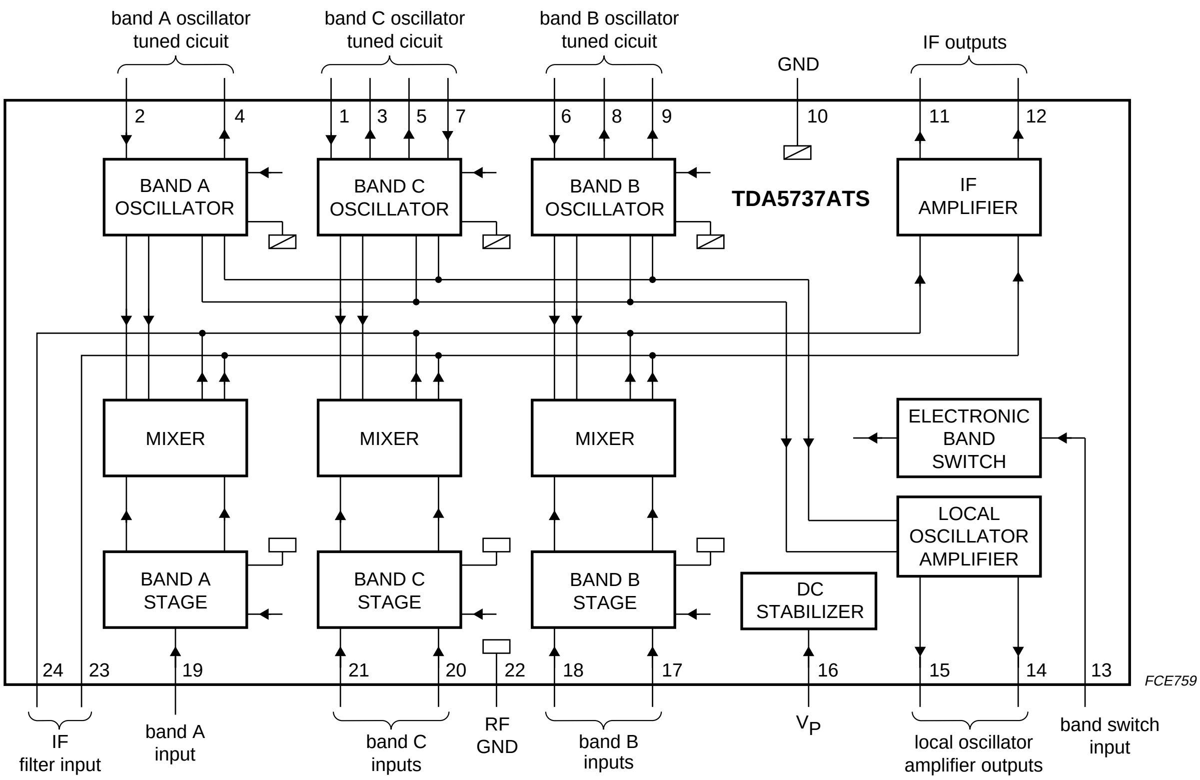


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
COSCIB2	1	band C oscillator input base 2
AOSCIB	2	band A oscillator input base
COSCOC2	3	band C oscillator output collector 2
AOSCOC	4	band A oscillator output collector
COSCOC1	5	band C oscillator output collector 1
BOSCIB	6	band B oscillator input base
COSCIB1	7	band C oscillator input base 1
BOSCOC2	8	band B oscillator output collector 2
BOSCOC1	9	band B oscillator output collector 1
GND	10	ground (0 V)
IFOUT2	11	IF amplifier output 2
IFOUT1	12	IF amplifier output 1
BS	13	band switch input
LOOUT2	14	local oscillator amplifier output 2
LOOUT1	15	local oscillator amplifier output 1
V_P	16	supply voltage
BIN2	17	band B input 2
BIN1	18	band B input 1
AIN	19	band A input
CIN2	20	band C input 2
CIN1	21	band C input 1
RFGND	22	ground for RF inputs
IFIN2	23	IF filter input 2
IFIN1	24	IF filter input 1

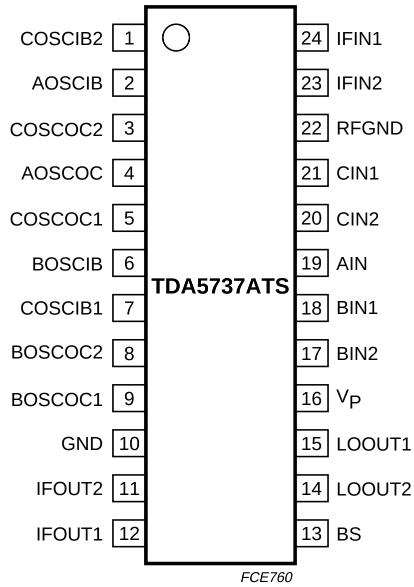


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	–0.3	+7.0	V
V_{SW}	switching voltage	–0.3	+7.0	V
$V_{n(max)}$	maximum voltage on each pin with a 22 kΩ resistor connected in series	–	35	V
I_O	output current of each pin to ground	–	–10	mA
$t_{sc(max)}$	maximum short-circuit time (all pins)	–	10	s
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	ambient temperature	–20	+80	°C
T_j	junction temperature	–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	120	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in circuit of Fig.16; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		4.5	5.0	5.5	V
I_P	supply current		42	50	58	mA
V_{SW}	switching voltage depending on supply voltage V_P	band A; note 1	0	–	$0.18V_P$	V
		band B; note 1	$0.26V_P$	–	$0.47V_P$	V
		band C; note 1	$0.55V_P$	–	V_P	V
I_{SW}	switching current	band A; note 1	–	–	2	µA
		band B; note 1	–	–	10	µA
		band C; note 1	–	–	25	µA
Band A mixer (including IF amplifier)						
$f_{i(RF)}$	RF input frequency	note 2	41	–	171	MHz
G_v	voltage gain	f_{RF} = 50 MHz; see Fig.3; note 3	20.5	23.0	25.5	dB
		f_{RF} = 170 MHz; see Fig.3; note 3	20.5	23.0	25.5	dB
NF	noise figure	f_{RF} = 50 MHz; see Figs.4 and 5	–	7.5	9	dB
		f_{RF} = 170 MHz; see Figs.4 and 5	–	9	10	dB
V_o	output voltage causing 1% cross modulation in channel	f_{RF} = 50 MHz; see Fig.6	115	118	–	dBµV
		f_{RF} = 170 MHz; see Fig.6	113	116	–	dBµV
V_i	input voltage level causing 10 kHz pulling in channel	f_{RF} = 170 MHz; note 4	96	100	–	dBmV
g_{os}	optimum source conductance for noise figure	f_{RF} = 50 MHz	–	0.5	–	mS
		f_{RF} = 170 MHz	–	1.1	–	mS
Y_i	input admittance	f_{RF} = 50 to 170 MHz; see Fig.11	–	0.3	–	mS
C_i	input capacitance	f_{RF} = 50 to 170 MHz; see Fig.11	–	1.9	–	pF
Band A oscillator						
f_{osc}	oscillator frequency	0.45 V < V_t < 28 V; notes 1 and 5	80	–	210	MHz
f_{shift}	frequency shift	ΔV_P = 5%; note 6	–	–	53	kHz
f_{drift}	frequency drift	no compensation				
		ΔT = 25 °C; NP0 capacitors; note 7	–	550	tbf	kHz
		5 s to 15 minutes after switch on; NP0 capacitors; note 8	–	150	tbf	kHz
		with compensation; see Fig.17				
		ΔT = 25 °C; notes 7 and 9	–	300	tbf	kHz
		5 s to 15 minutes after switch on; notes 8 and 9	–	20	tbf	kHz
$V_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	4.75 V < V_P < 5.25 V; see Fig.7				
		f_{osc} = 80 MHz	20	–	–	mV
		f_{osc} = 210 MHz	20	–	–	mV
Φ_N	phase noise	measured at the IF output at 10 kHz offset; V_o = 105 dBµV	81	–	–	dBc/Hz

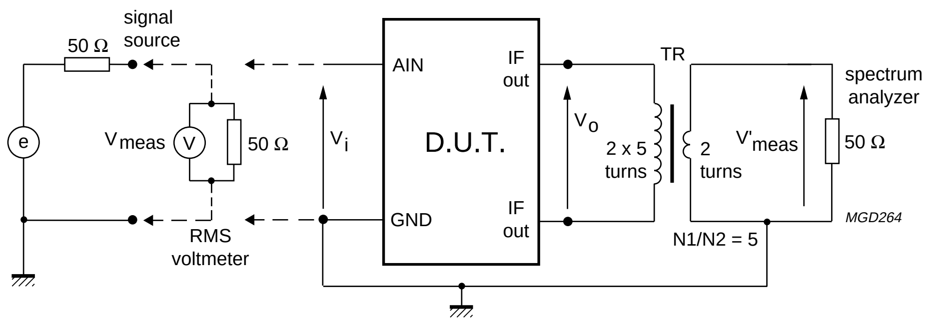
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band B mixer (including IF amplifier)						
$f_{i(RF)}$	RF input frequency	note 2	166	–	451	MHz
G_v	voltage gain	f_{RF} = 170 MHz; see Fig.8; note 3	31	34	37	dB
		f_{RF} = 450 MHz; see Fig.8; note 3	31	34	37	dB
NF	noise figure (not corrected for image)	f_{RF} = 170 MHz; see Fig.9	–	8	10	dB
		f_{RF} = 450 MHz; see Fig.9	–	8	10	dB
V_o	output voltage causing 1% cross modulation in channel	f_{RF} = 170 MHz; see Fig.10	114	117	–	dBμV
		f_{RF} = 450 MHz; see Fig.10	112	115	–	dBμV
V_i	input voltage level causing 10 kHz pulling in channel	f_{RF} = 450 MHz; note 4	83	87	–	dBμV
R_S	real part of output impedance Z_o ($R_S + j\omega L_S$)	f_{RF} = 170 to 450 MHz; see Fig.12	–	23	–	Ω
L_S	imaginary part of output impedance Z_o ($R_S + j\omega L_S$)	f_{RF} = 170 to 450 MHz; see Fig.12	–	9	–	nH
Band B oscillator						
f_{osc}	oscillator frequency	0.45 V < V_t < 28 V; notes 1 and 5	205	–	490	MHz
f_{shift}	frequency shift	ΔV_P = 5%; note 6	–	–	53	kHz
f_{drift}	frequency drift	no compensation				
		ΔT = 25 °C; NP0 capacitors; note 7	–	2500	tbf	kHz
		5 s to 15 minutes after switch on; NP0 capacitors; note 8	–	900	tbf	kHz
		with compensation; see Fig.17				
		ΔT = 25 °C; notes 7 and 9	–	400	tbf	kHz
		5 s to 15 minutes after switch on; notes 8 and 9	–	65	tbf	kHz
$V_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	4.75 V < V_P < 5.25 V; see Fig.7				
		f_{osc} = 250 MHz	20	–	–	mV
		f_{osc} = 490 MHz	20	–	–	mV
Φ_N	phase noise	measured at the IF output at 10 kHz offset; V_o = 105 dBmV	81	–	–	dBc/Hz
Band C mixer (including IF amplifier)						
$f_{i(RF)}$	RF input frequency	note 2	446	–	861	MHz
G_v	voltage gain	f_{RF} = 450 MHz; see Fig.8; note 3	31	34	37	dB
		f_{RF} = 860 MHz; see Fig.8; note 3	31	34	37	dB
NF	noise figure (not corrected for image)	f_{RF} = 450 MHz; see Fig.9	–	9	11	dB
		f_{RF} = 860 MHz; see Fig.9	–	9	11	dB
V_o	output voltage causing 1% cross modulation in channel	f_{RF} = 450 MHz; see Fig.10	112	115	–	dBμV
		f_{RF} = 860 MHz; see Fig.10	112	115	–	dBμV
V_i	input voltage level causing 10 kHz pulling in channel	f_{RF} = 860 MHz; note 4	91	95	–	dBμV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_S	real part of output impedance Z_o (R_S + jωL_S)	f_{RF} = 450 to 860 MHz; see Fig.13	–	28	–	Ω
L_S	imaginary part of output impedance Z_o (R_S + jωL_S)	f_{RF} = 450 to 860 MHz; see Fig.13	–	10	–	nH
Band C oscillator						
f_{osc}	oscillator frequency	0.45 V < V_t < 28 V; notes 1 and 5	485	–	900	MHz
f_{shift}	frequency shift	ΔV_P = 5%; note 6	–	–	53	kHz
f_{drift}	frequency drift	no compensation				
		ΔT = 25 °C; NP0 capacitors; note 7	–	3100	tbf	kHz
		5 s to 15 minutes after switch on; NP0 capacitors; note 8	–	650	tbf	kHz
		with compensation; see Fig.17				
		ΔT = 25 °C; notes 7 and 9	–	1200	tbf	kHz
		5 s to 15 minutes after switch on; notes 8 and 9	–	120	tbf	kHz
$V_{ripple(p-p)}$	ripple susceptibility of supply voltage (peak-to-peak value)	4.75 V < V_P < 5.25 V; see Fig.7				
		f_{osc} = 485 MHz	20	–	–	mV
		f_{osc} = 900 MHz	18	–	–	mV
Φ_N	phase noise	measured at the IF output at 10 kHz offset; V_o = 105 dBμV	81	–	–	dBc/Hz
IF amplifier						
s_{22}	output reflection coefficient	magnitude; see Fig.14	–	–16	–	dB
		phase; see Fig.14	–	12	–	deg.
R_S	real part of output impedance Z_o (R_S + jωL_S)		–	67	–	Ω
L_S	imaginary part of output impedance Z_o (R_S + jωL_S)		–	20	–	nH
LO output						
Y_o	output admittance (Y_P + jωC_P)	f_{RF} = 80 MHz; see Fig.15	–	2.5	–	mS
		f_{RF} = 900 MHz; see Fig.15	–	5	–	mS
C_P	imaginary part of output admittance Y_o (Y_P + jωC_P)	see Fig.15	–	0.9	–	pF
V_o	output voltage	R_L = 50 Ω; 0 < V_t < 35 V	80	91	100	dBμV
SRF	spurious signal on LO output with respect to LO output signal	R_L = 50 Ω; 0.2 V < V_t < 35 V; notes 1 and 10	–	–	–10	dB
HLO	LO signal harmonics with respect to LO signal	R_L = 50 Ω; 0 < V_t < 35 V; note 1	–	–	–10	dB

Notes

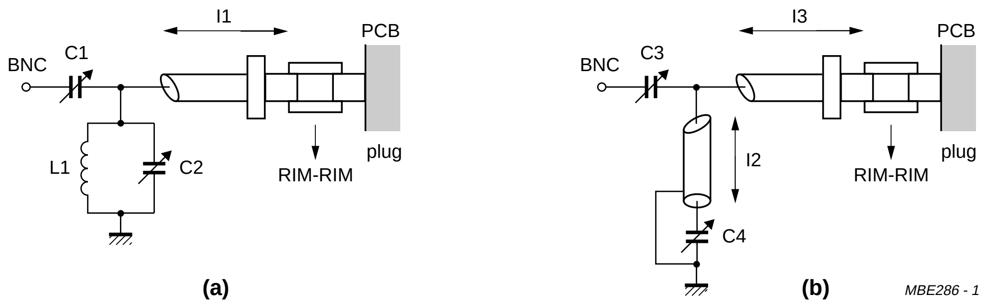
1. –20 °C < T_{amb} < +80 °C; 4.5 V < V_P < 5.5 V.
2. The RF frequency range is defined by the oscillator frequency range and the intermediate frequency.

3. The gain is defined as the transducer gain (measured in Fig.16) plus the voltage transformation ratio of L7 to L8 (10 : 2 and 15.4 dB including transformer loss).
4. The input level causing 10 kHz frequency detuning at the LO output. $f_{osc} = f_{RF} + 33.4$ MHz.
5. Limits are related to the tank circuits used in Fig.16. Frequency bands may be adjusted by the choice of external components.
6. The frequency shift is defined as the change in oscillator frequency when the supply voltage varies from $V_P = 5$ to 4.75 V and from $V_P = 5$ to 5.25 V.
7. The frequency drift is defined as the change in oscillator frequency when the ambient temperature varies from $T_{amb} = 25$ to 0 °C and from $T_{amb} = 25$ to 50 °C.
8. Switch-on drift is defined as the change in oscillator frequency between 5 s and 15 minutes after switch on.
9. With thermal compensation, the capacitors of the tank circuits have the following temperature coefficients:
   a) In band A: C1, C6 and C8 are N750
   b) In band B: C4, C11, C12, C13 and C36 are N750
   c) In band C: C5, C7, C9 and C10 are N750; C2 is N220 and C3 is NP0.
10. SRF: spurious signal on LO with respect to LO output signal:
    a) RF level = 120 dBμV at $f_{RF} < 180$ MHz
    b) RF level = 107.5 dBμV at $f_{RF} = 180$ to 225 MHz
    c) RF level = 97 dBμV at $f_{RF} = 225$ to 860 MHz.



$Z_{i(AIN)} >> 50\ \Omega$; $V_i = 2 \times V_{meas}$.
$V_i = V_{meas} + 6$ dB.
$V_o = V'_{meas} + 15.4$ dB (transformer ratio N1/N2 = 5 and transformer loss).
$G_v = 20 \log (V_o/V_i)$.

Fig.3 Band A gain measurement.



(a) For f_{RF} = 50 MHz:
mixer A frequency response measured = 57 MHz; loss = 0 dB
image suppression = 16 dB.

C1 = 9 pF

C2 = 15 pF

L1 = 7 turns (diameter = 5.5 mm; wire diameter = 0.5 mm)

I1 = semi rigid cable (RIM): 5 cm long (semi rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

(b) For f_{RF} = 150 MHz:
mixer A frequency response measured = 150.3 MHz; loss = 1.3 dB
image suppression = 13 dB.

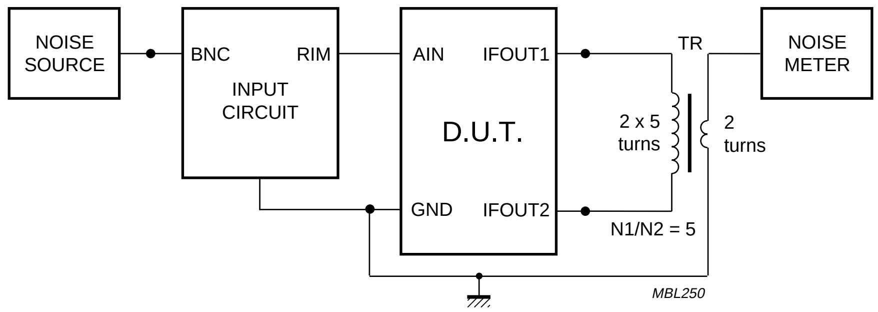
C3 = 5 pF

C4 = 25 pF

I2 = semi rigid cable (RIM): 30 cm long

I3 = semi rigid cable (RIM): 5 cm long (semi rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

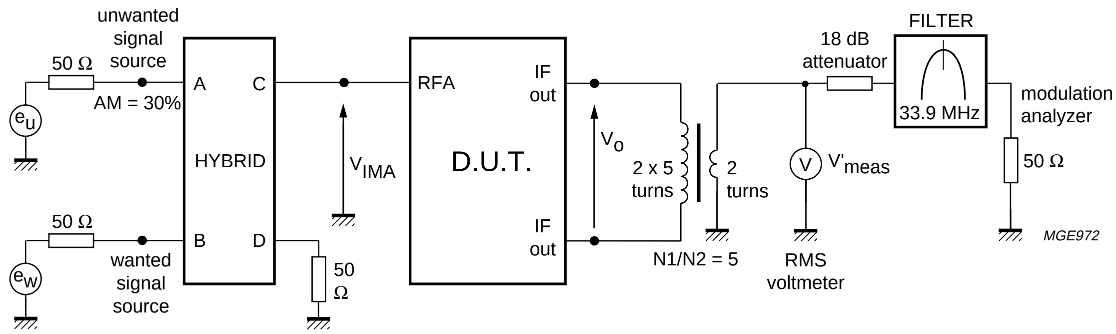
Fig.4 Input circuit for optimum noise figure in band A.



See Fig.4 for input circuit.

$NF = NF_{meas}$ – loss (input circuit) dB.

Fig.5 Noise figure measurement in band A.



$V'_{meas} = V_o$ – 15.4 dB (transformer ratio N1/N2 = 5 and transformer loss).

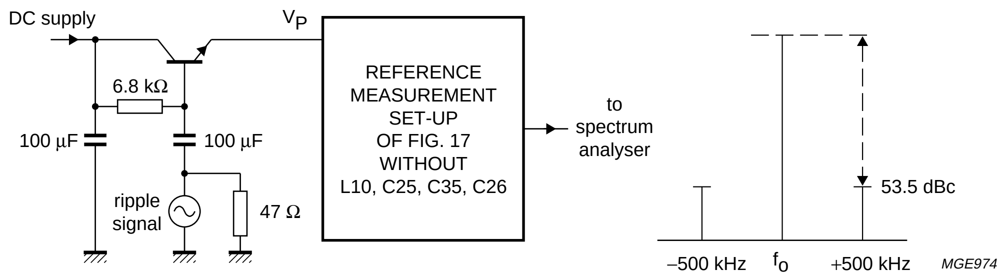
Wanted output signal at f_{RFW} = 50 MHz (170 MHz); V_{ow} = 80 dBμV.

We measure the level of the unwanted signal V_{ou} causing 1% AM modulation in the wanted output signal; f_{RFU} = 45.5 MHz (165.5 MHz); f_{osc} = 83.9 MHz (203.9 MHz).

$V_{ou} = V'_{meas}$ + 15.4 dB.

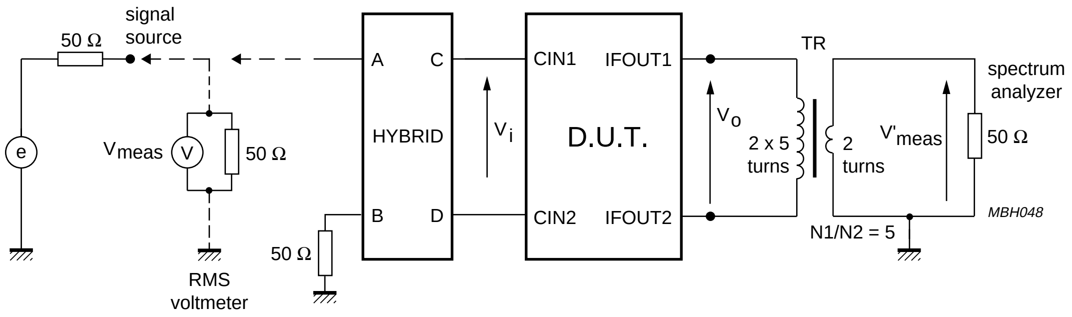
Filter characteristics: f_c = 33.9 MHz; f_{-3dBBW} = 1 MHz; $f_{-30dBBW}$ = 2.3 MHz.

Fig.6 Cross modulation measurement in band A.



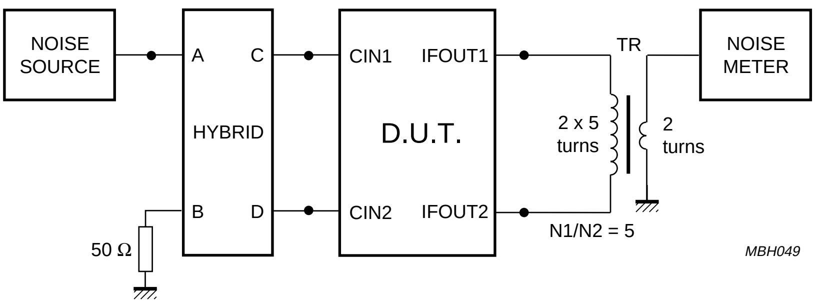
The ripple susceptibility is defined as the level of a signal added to the supply voltage causing sidebands in the LO output at 53.5 dBc.
This signal has a frequency between 20 Hz and 500 kHz.

Fig.7 Ripple susceptibility.



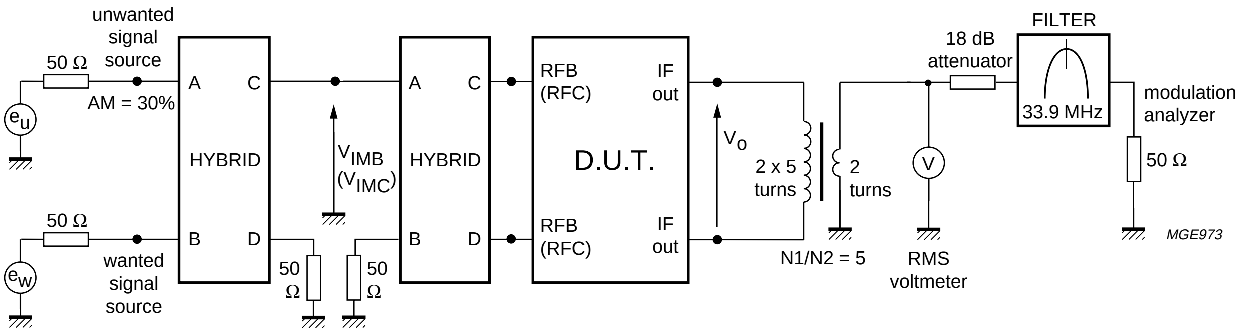
$loss_{(hybrid)}$ = 1 dB.
$V_i = V_{meas} - loss_{(hybrid)}$.
$V_o = V'_{meas}$ + 15.4 dB (transformer ratio N1/N2 and transformer loss).
Voltage gain for band B and C = 20 log (V_o/V_i).

Fig.8 Gain measurement in bands B and C.



Loss of the hybrid: 1 dB.
$NF = NF_{meas}$ – loss of the hybrid.

Fig.9 Noise figure measurement in bands B and C.



$V'_{meas} = V_o - 15.4$ dB (transformer ratio N1/N2 = 5 and transformer loss).

Wanted output signal at f_{RFW} = 170 or 450 MHz (450 or 860 MHz); V_{ow} = 70 dBμV.

We measure the level of the unwanted signal V_{ou} causing 1% AM modulation in the wanted output signal; f_{RFU} = 165.5 or 445.5 MHz (445.5 or 855.5 MHz); f_{OSC} = 203.9 or 483.9 MHz (483.9 or 893.9 MHz).

$V_{ou} = V'_{meas} + 15.4$ dB.

Filter characteristics: f_c = 33.9 MHz; f_{-3dBBW} = 1 MHz; $f_{-30dBBW}$ = 2.3 MHz.

Fig.10 Cross modulation measurement in bands B and C.

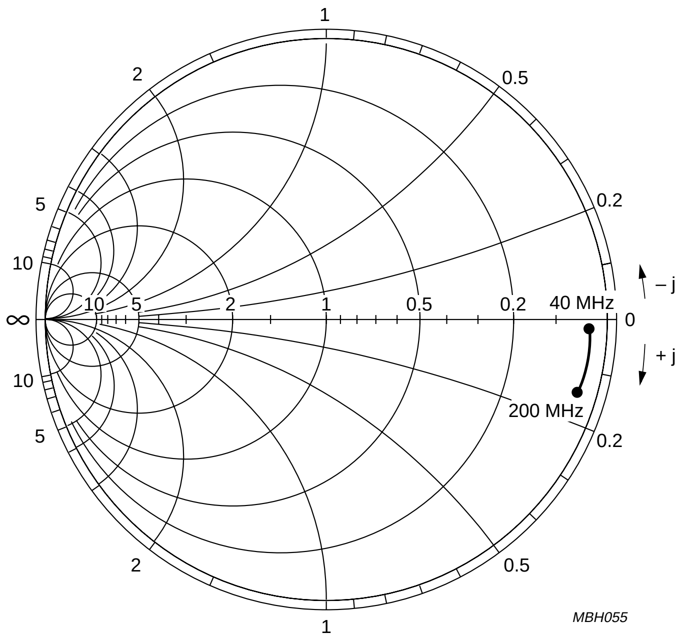


Fig.11 Input admittance (s_{11}) of the band A mixer input (40 to 200 MHz); Y_o = 20 mS.

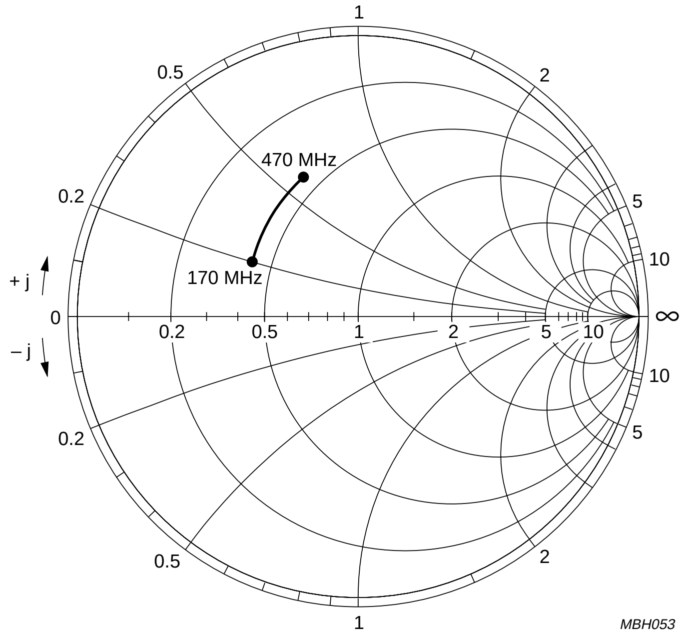


Fig.12 Input impedance (s_{11}) of the band B mixer input (170 to 470 MHz); Z_o = 50 Ω.

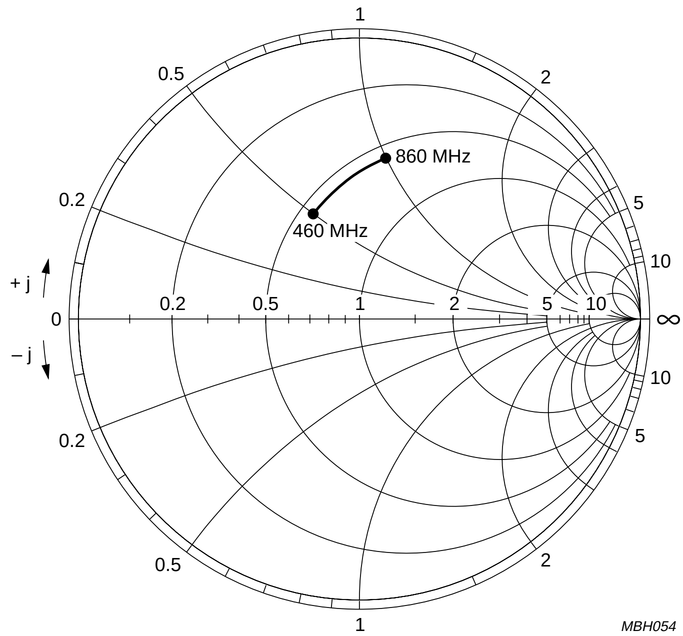


Fig.13 Input impedance (s_{11}) of the band C mixer input (460 to 860 MHz); Z_o = 50 Ω.

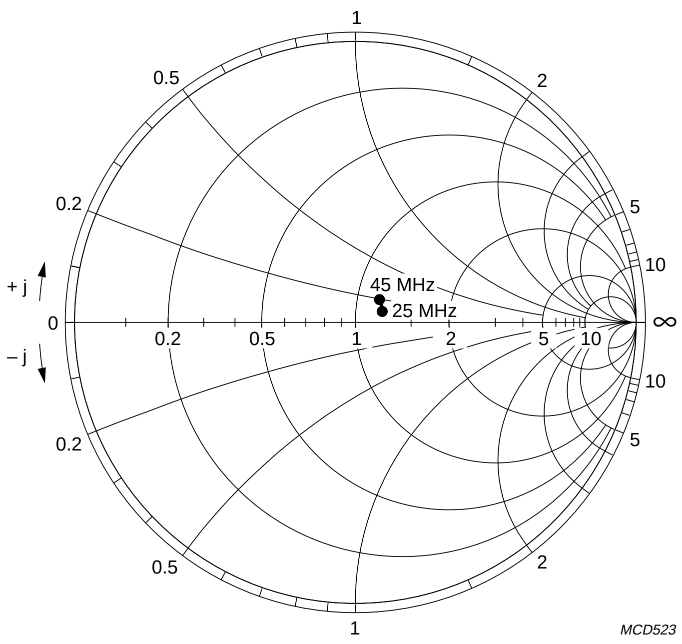


Fig.14 Output impedance (s_{22}) of the IF amplifier (25 to 45 MHz); Z_o = 100 Ω.

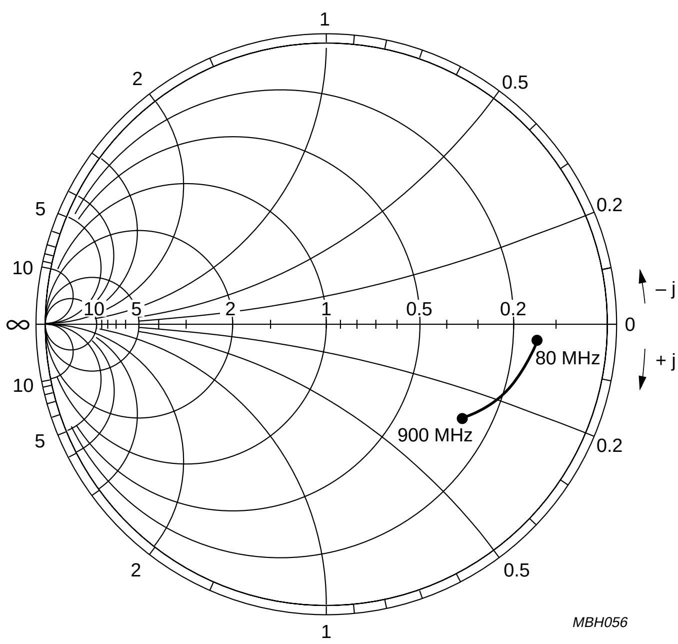
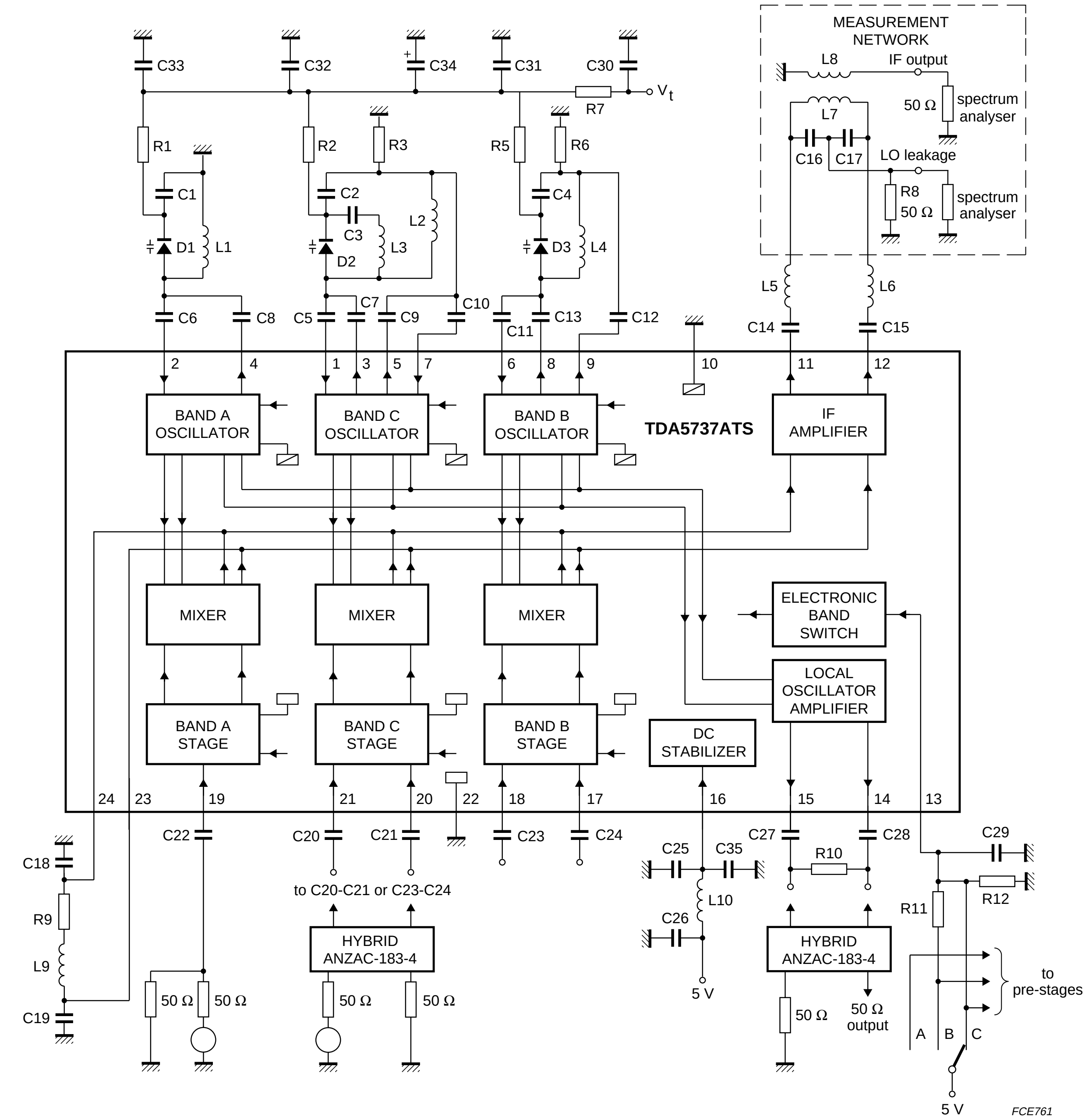


Fig.15 Output admittance (s_{22}) of the LO amplifier (80 to 900 MHz); Y_o = 20 mS.

APPLICATION INFORMATION



L7, L8, C16, C17 and R8 are only necessary for measurements (these components are not used in a tuner).

Fig.16 Measurement circuit.

Table 1 Capacitors of Fig.16 (all SMD and NP0 except C34 and C35)

NUMBER	VALUE
C1	82 pF
C2	5.6 pF
C3	100 pF
C4	82 pF
C5	1 pF
C6	2 pF
C7	2 pF
C8	2 pF
C9	2 pF
C10	1 pF
C11	3.3 pF
C12	3.3 pF
C13	4.7 pF
C14	1 nF
C15	1 nF
C16	39 pF
C17	39 pF
C18	68 pF
C19	68 pF
C20	1 nF
C21	1 nF
C22	1 nF
C23	1 nF
C24	1 nF
C25	2.2 nF
C26	1 nF
C27	1 nF
C28	1 nF
C29	1 nF
C30	1 nF
C31	1 nF
C32	1 nF
C33	1 nF
C34	2.2 µF; 40 V electrolytic
C35	4.7 nF

Table 2 Resistors of Fig.16 (all SMD)

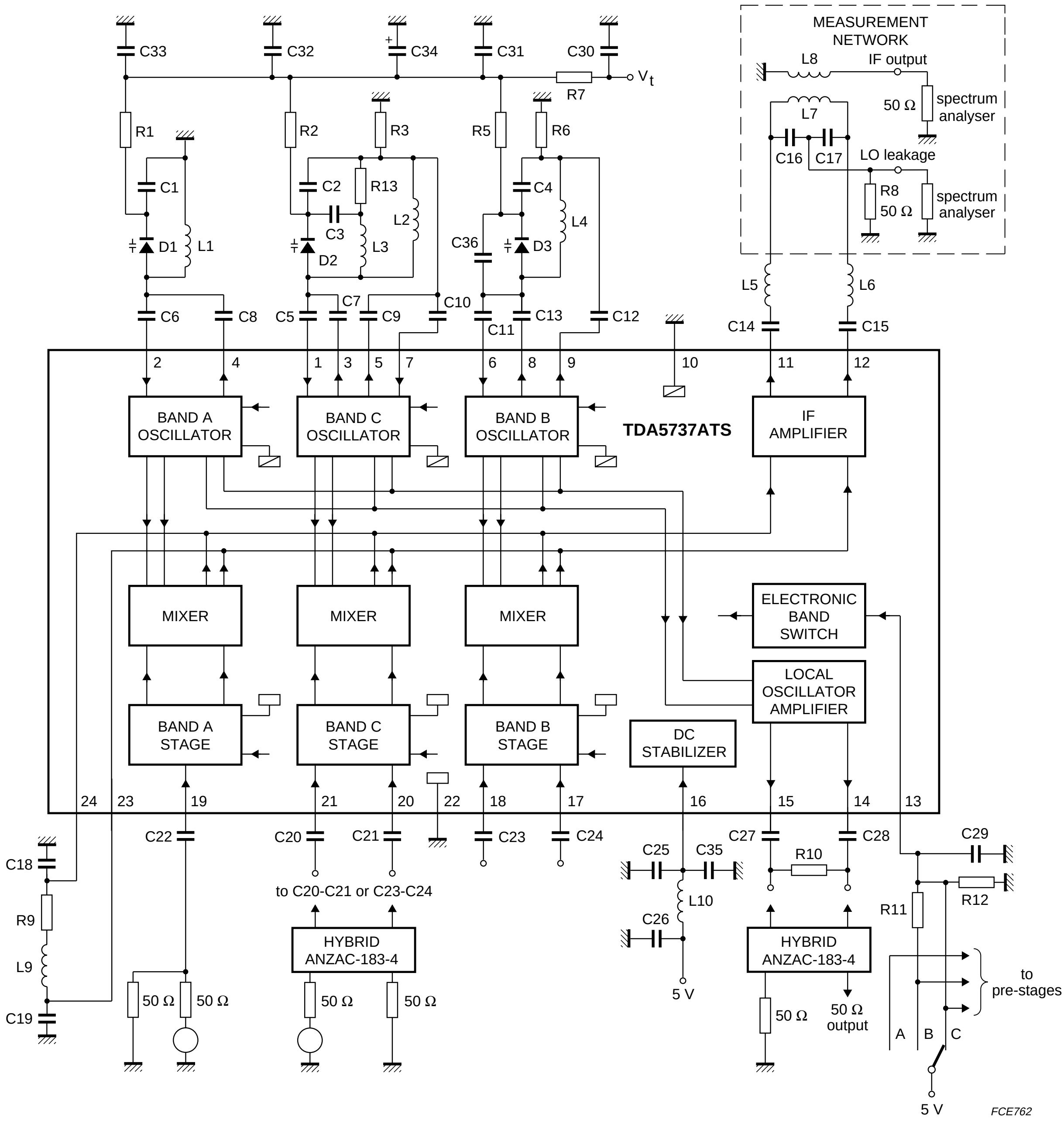
NUMBER	VALUE
R1	47 kΩ
R2	22 kΩ
R3	22 kΩ
R5	27 kΩ
R6	27 kΩ
R7	10 kΩ
R8	50 Ω
R9	4.7 Ω
R10	100 Ω
R11	27 kΩ
R12	15 kΩ

Table 3 Diodes, coils and transformers of Fig.16

NUMBER	VALUE
Diodes	
D1	BB132
D2	BB134
D3	BB133
Coils; note 1	
L1	7.5 turns (∅ 3 mm)
L2	2.5 turns (∅ 3.5 mm)
L3	1.5 turns (∅ 2.5 mm)
L4	2.5 turns (∅ 3 mm)
L5	5.5 turns (∅ 2.5 mm)
L6	5.5 turns (∅ 2.5 mm)
L9	12.5 turns (∅ 5 mm)
L10	2.2 µH (choke coil)
Transformers; note 2	
L7	2 × 5 turns
L8	2 turns

Notes

1. Wire size for L1 to L6 is 0.4 mm.
2. Coil type: TOKO 7kL.



L7, L8, C16, C17 and R8 are only necessary for measurements (these components are not used in a tuner).

Fig.17 Measurement circuit with thermal compensation.

Table 4 Capacitors of Fig.17 (all SMD except C34)

NUMBER	VALUE
C1	62 pF
C2	6 pF
C3	100 pF
C4	68 pF
C5	1.2 pF
C6	2 pF
C7	1.2 pF
C8	2 pF
C9	1.5 pF
C10	1.5 pF
C11	3 pF
C12	3 pF
C13	4.3 pF
C14	1 nF
C15	1 nF
C16	39 pF
C17	39 pF
C18	68 pF
C19	68 pF
C20	1 nF
C21	1 nF
C22	1 nF
C23	1 nF
C24	1 nF
C25	2.2 nF
C26	1 nF
C27	1 nF
C28	1 nF
C29	1 nF
C30	1 nF
C31	1 nF
C32	1 nF
C33	1 nF
C34	2.2 μF; 40 V electrolytic
C35	4.7 nF
C36	0.5 pF

Table 5 Resistors of Fig.17 (all SMD)

NUMBER	VALUE
R1	47 kΩ
R2	22 kΩ
R3	22 kΩ
R5	27 kΩ
R6	27 kΩ
R7	10 kΩ
R8	50 Ω
R9	4.7 Ω
R10	100 Ω
R11	27 kΩ
R12	15 kΩ
R13	4.7 kΩ

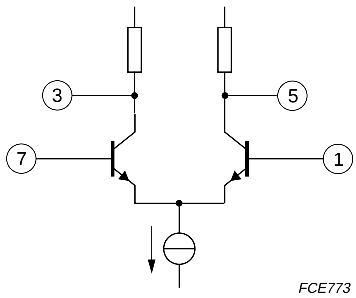
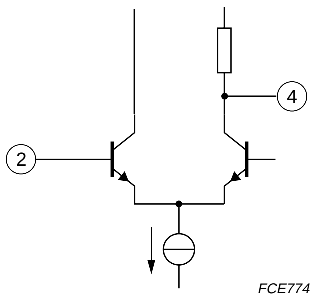
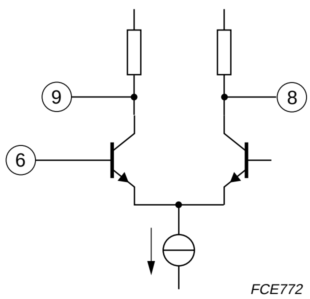
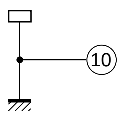
Table 6 Diodes, coils and transformers of Fig.17

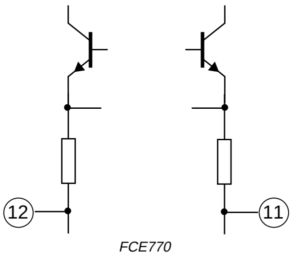
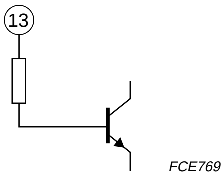
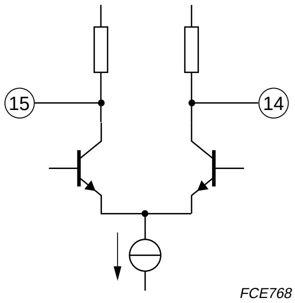
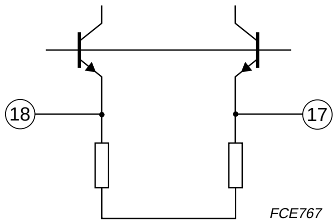
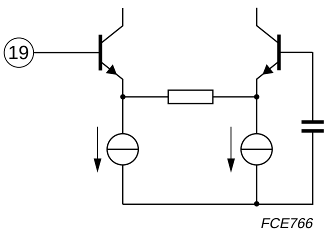
NUMBER	VALUE
Diodes	
D1	BB132
D2	BB134
D3	BB133
Coils; note 1	
L1	7.5 turns (∅ 3 mm)
L2	2.5 turns (∅ 2 mm)
L3	2.5 turns (∅ 2 mm)
L4	2.5 turns (∅ 2.5 mm)
L5	5.5 turns (∅ 2.5 mm)
L6	5.5 turns (∅ 2.5 mm)
L9	12.5 turns (∅ 5 mm)
L10	2.2 μH; choke coil
Transformers; note 2	
L7	2 × 5 turns
L8	2 turns

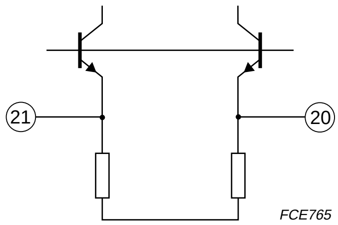
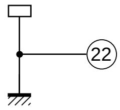
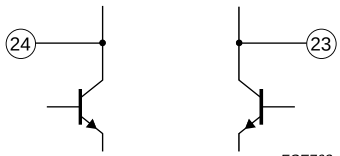
Notes

1. The wire size for L1, L2, L5 and L6 is 0.4 mm; the wire size for L3 and L4 is 0.5 mm.
2. Coil type: TOKO 7kL.

INTERNAL PIN CONFIGURATION

SYMBOL	PIN	DESCRIPTION	AVERAGE DC VOLTAGE (V)(1)(2)		
			BAND A	BAND B	BAND C
COSCIB2	1	 FCE773	NR	NR	2.0
COSCOC2	3		NR	NR	2.7
COSCOC1	5		NR	NR	2.7
COSCIB1	7		NR	NR	2.0
AOSCIB	2	 FCE774	2.0	NR	NR
AOSCOC	4		2.5	NR	NR
BOSCIB	6	 FCE772	NR	2.0	NR
BOSCOC2	8		NR	2.7	NR
BOSCOC1	9		NR	2.7	NR
GND	10	 FCE771	0.0	0.0	0.0

SYMBOL	PIN	DESCRIPTION	AVERAGE DC VOLTAGE (V)(1)(2)		
			BAND A	BAND B	BAND C
IFOUT2	11		2.1	NR	NR
IFOUT1	12		2.1	NR	NR
BS	13		0.0	1.8	5.0
LOOUT2	14		4.2	NR	NR
LOOUT1	15		4.2	NR	NR
V_P	16	supply voltage	5.0	5.0	5.0
BIN2	17		NR	1.0	NR
BIN1	18		NR	1.0	NR
AIN	19		1.8	NR	NR

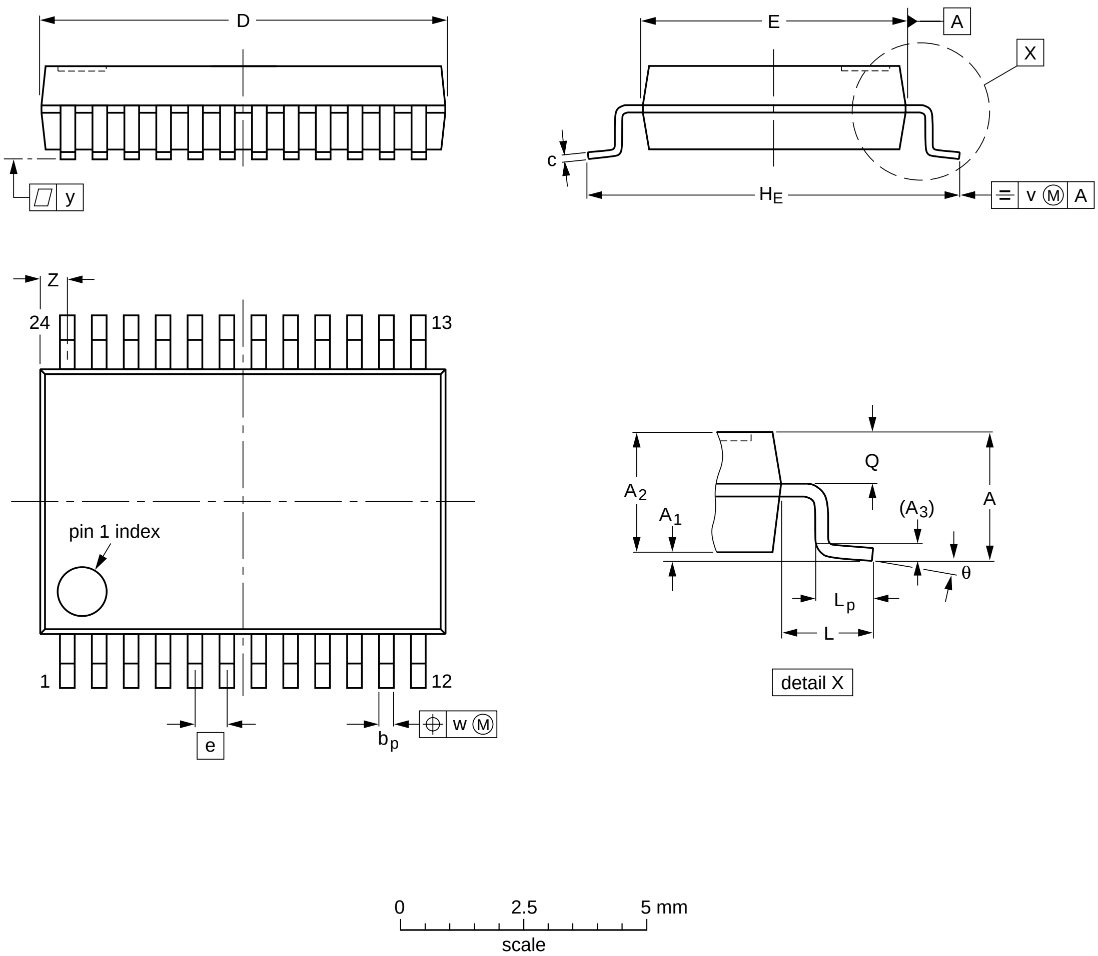
SYMBOL	PIN	DESCRIPTION	AVERAGE DC VOLTAGE (V)(1)(2)		
			BAND A	BAND B	BAND C
CIN2	20	 FCE765	NR	NR	1.0
CIN1	21		NR	NR	1.0
RFGND	22	 FCE764	0	0	0
IFIN2	23	 FCE763	3.6	3.6	3.6
IFIN1	24		3.6	3.6	3.6

Notes

1. NR = not relevant.
2. Measured in circuit shown in Fig.16.

PACKAGE OUTLINE

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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